CLAIMS:

1. A controllable amplifier arrangement comprising

- a first differential amplifier stage having a first and a second output branch,
- a second differential amplifier stage which is coupled to the first output branch of the first differential amplifier stage and has at least a first and a second output branch, at which a first current in the first output branch of the first differential amplifier stage is controllably divided into partial currents,
- a third differential amplifier stage which is coupled to the second output branch of the first differential amplifier stage and has at least a first and a second output branch, at which a second current in the second output branch of the first differential amplifier stage is controllably divided into partial currents,
- a first load impedance coupled to one of the first output branches of the second differential amplifier stage for generating a first output voltage from the partial current flowing in said one of the first output branches of the second differential amplifier stage, and
- a second load impedance coupled to one of the first output branches of the third differential amplifier stage for generating a second output voltage from the partial current flowing in said one of the first output branches of the third differential amplifier stage,

wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively.

2. A controllable amplifier arrangement as claimed in claim 1, characterized in that said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the first load impedance, and in that said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the second load impedance.

3. A controllable amplifier arrangement as claimed in claim 1, characterized in that said one of the second output branches of the second differential amplifier stage is coupled to a tap on the first load impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap on the second load impedance.

4. An arrangement for processing electric signals, characterized by at least one controllable amplifier arrangement as claimed in any one of the preceding claims.

5. An arrangement as claimed in claim 4, comprising at least two controllable amplifier arrangements as claimed in any one of claims 1 to 3, characterized in that the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals.

6. An arrangement as claimed in claim 5, characterized in that the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements.